CLAIMS

What is claimed is:

1. A maximum likelihood bit synchronizer for use in a communication system including a transmitter that generates a transmitter signal at a first rate and a receiver that samples the transmitter signal at a higher rate than the first rate and generates a receiver signal, said synchronizer comprising:

a tapped delay line;

n timing hypothesis circuits coupled to said tapped delay line, wherein n is an integer equal to the sampling rate divided by said first rate plus two; and

a control and adjudication circuit coupled to said n timing hypothesis circuits that compares outputs of said n timing hypothesis circuits and selects one of said n timing hypothesis circuits.

2. The synchronizer of claim 1 further comprising an antipodal circuit coupled to an input of said tapped delay line for generating an antipodal signal from said receiver signal.

3. The synchronizer of claim 2 wherein said antipodal circuit includes an average level estimator.

4. The synchronizer of claim 3 wherein said antipodal circuit further includes a summing circuit that receives said antipodal signal and said receiver signal and that generates said antipodal signal.

5. The synchronizer of claim 1 wherein the receiver signal is a general bilevel signal independent of modulation type.

6. The synchronizer of claim 1 wherein the transmitter signal is selected from the group consisting of on-off keyed signals and FSK signals.

7. The synchronizer of claim 1 wherein said tapped delay line includes n plus 2 delay elements.

8. The synchronizer of claim 1 wherein each of said n timing hypothesis circuits includes a sum-and-dump summer connected to (n-2) outputs of said tapped delay line.

9. The synchronizer of claim 8 wherein each of said n timing hypothesis circuits further includes an absolute value circuit that is connected to said sum-and-dump summer.

10. The synchronizer of claim 9 wherein each of said n timing hypothesis circuits further includes an averaging circuit.

11. The synchronizer of claim 10 wherein said averaging circuit is a sliding window summer.

12. The synchronizer of claim 11 wherein said averaging circuit is a single pole, unity gain, low-pass filter.

13. The synchronizer of claim 8 further comprising a select switch coupled to said sum-and-dump summers, wherein said select switch receives a switch control signal from said control and adjudication circuits that selects an output signal of one of said sum-and-dump summers.

14. The synchronizer of claim 13 further comprising a threshold test circuit that compares said selected output signal to a threshold value and outputs one of a mark symbol or a space symbol.

15. The synchronizer of claim 14 further comprising an output control circuit that receives an output control signal from said control and adjudication circuit, wherein said output control circuit outputs zero, one or two mark or space signals in response to said output control signal.

16. A maximum likelihood bit synchronizer coupled to a receiver that generates a receiver signal, comprising:

an average level estimator coupled to said receiver signal that generates an average signal;

a summing circuit coupled to said receiver signal and said average signal and that outputs an antipodal signal;

a tapped delay line coupled to said summing circuit;

a plurality of timing hypothesis circuits coupled to said tapped delay line, wherein each of said timing hypothesis circuits include a data detector, an absolute value circuit connected to said data detector, and an averaging circuit connected to said absolute value circuit; and

a control and adjudication circuit coupled to said timing hypothesis circuits that compares outputs of said timing hypothesis circuits and selects one of said timing hypothesis circuits.

17. The maximum likelihood bit synchronizer of claim 16 wherein n timing hypothesis circuits are provided and wherein n is the greatest integer that is equal to a symbol rate divided by a sampling rate plus 2.

18. The maximum likelihood bit synchronizer of claim 16 further comprising a select switch connected to said data detectors of said timing hypothesis circuits and to said control and adjudication circuit.

19. The maximum likelihood bit synchronizer of claim 18 further comprising:

a threshold test circuit that compares said selected signal to a threshold value and outputs one of a mark symbol and a space symbol; and

an output control circuit that outputs zero, one or two mark or space symbols.

20. The maximum likelihood bit synchronizer of claim 16 wherein the receiver signal is a general bilevel signal independent of modulation type.

21. The maximum likelihood bit synchronizer of claim 16 wherein said receiver signal is selected from the group consisting of on-off keyed signals and FSK signals.

22. The maximum likelihood bit synchronizer of claim 16 wherein said tapped delay line includes (n+2) delay elements.

23. The maximum likelihood bit synchronizer of claim 16 wherein said data detector is a sum-and-dump summer connected to (n-2) outputs of said tapped delay line.

24. The maximum likelihood bit synchronizer of claim 16 wherein said averaging circuit is a sliding window summer.

25. The maximum likelihood bit synchronizer of claim 16 wherein said averaging circuit is a single pole, unity gain, low-pass filter.

26. The maximum likelihood bit synchronizer of claim 18 wherein said control and adjudication circuit outputs a switch control signal to said select switch to select an output of one of said data detectors and an output control signal to said output control circuit to select output of zero, one or two mark or space symbols.